REMARKS

This responds to the Office Action mailed on April 14, 2006.

Claims 1 and 8 are amended, claims 2, 9 and 10 are canceled, and claims 12-18 are added; as a result, claims 1, 3-8, 11-18 are now pending in this application.

§103 Rejection of the Claims

Claims 1-3 and 5-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Schimmel (US 6,105,113), and in view of Fossum et al. (US 4,888,679).

Schimmel describes a system and method for maintaining translation look-aside buffer (TLB) consistency. Schimmel specifically describes a computer system comprising: a network and one or more processing nodes connected via the network, wherein each processing node includes: a plurality of processors and a shared memory connected to each of the processors.

Fossum describes an apparatus comprising a vector processor and a scalar processor, where the scalar processor and the vector processor operate independently of each other by using a cache.

None of the cited references, however, teach or suggest a computer system taught by Applicant and claimed in claims 1, 3, 5-8 and 11. For example, neither Schimmel nor Fossum teach or suggest translating virtual memory addresses received from other processing nodes into physical addresses within the shared memory of a first processing node as taught by Applicant and claimed in claims 1 and 8.

The Examiner argues that Schimmel discloses this limitation and then points to col. 7, lines 1-7, col. 9, lines 20-29 and Fig. 5-9. Although these cited portions describe a translation process in case of a TLB miss, the structures of page tables required for address translation and the relevant steps for translation, they do not teach or suggest the translating approach described and claimed by Applicant.

For example, Schimmel states that if the page table entry address in main memory (810) [of one node] does not store a valid physical address, the system will have to access external memory devices to bring the data into main memory (810) and update an appropriate PTE (Page Table Entry) with the physical address of the data (Col. 10, lines 57-67). Schimmel further states

that the PTE and the PTE address are sent to processor and cache node (410) and stored in cache (416) [of the same node]. *Id.*

This contrasts with the translation approach under Applicant's invention that sends virtual addresses to the appropriate remote nodes and lets each of the remote nodes translate the virtual memory address into a physical memory address within the shared memory of the remote node via a RTT (Remote Address Translation) on the remote node as described and claimed by Applicant.

In addition, neither Schimmel nor Fossum teach or suggest having processors on one node load data directly from and store data directly to shared memory on another processing node via addresses that are translated on the other processing node using the other processing node's RTT as described and claimed by Applicant.

Claims 1 and 8 have been amended to emphasize these differences. Reconsideration is respectfully requested.

With regard to claim 6, claim 6 is patentable as being dependent on a patentable base claim. In addition, neither Schimmel nor Fossum teach or suggest a scalar processing unit including a scalar cache memory which contains a subset of cache lines stored in the shared memory cache as taught by Applicant and claimed in claim 6.

The Examiner argues that Fossum discloses this limitation and then points to Fig. 1 and col. 4, lines 15-54. The cache in Fig. 1 describes a cache device (24) associated and shared by the scalar (21) and vector (22) processing units. Col. 4, lines 15-54 describes the principle of locality and the necessary elements of the cache device to process data by block. Alone or in combination, however, the cited portions do not teach or suggest a scalar cache memory containing a subset of cache lines stored in the shared memory cache as described and claimed by Applicant.

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Schimmel (US 6,105,113), in view of Fossum et al. (US 4,888,679), and further in view of of Nakazato (US 6,782,468). Claim 4 is, however, patentable as being dependent on a patentable base claim. In

addition, none of the cited references does not teach or suggest a processor including two vector pipelines as described and claimed by Applicant.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 3 day of August 2006.

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